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[TITLE OF THE INVENTION]

Method of Manufacturing MOS Semiconductor Device

[ABSTRACT]

[PROBLEM TO BE SOLVED]

To form a high Vth MOSFET and a low Vth MOSFET respectively including gate insulating films of different kinds of thickness without coverage over the gate insulating films with resist.

[SOLUTION]

A silicon oxide film 3 over a low Vth region is removed with the etching process (b) and a nitride film 4 is formed (c) over the low Vth region with the nitridation process. The silicon oxide film 3 over a high Vth region is removed (d) with

the etching process without formation of a resist film. A semiconductor substrate 1 is thermally oxidized to form (e) a thick gate insulating film (5) over the high Vth region and a thin gate insulating film (6) over the low Vth region. A gate electrode is formed and an impurity diffusing layer 8 which will become a source and drain region is also formed (f).

[CLAIMS]

[Claim 1]

A method of manufacturing MOS semiconductor device comprising the steps of:

(1) covering respectively a first active region and a second active region segmented with an element isolating and insulating film with a first insulating film;

(2) removing selectively the first insulating film over the first active region with the etching process;

(3) forming a second insulating film over the first active region with a material having the etching property which is different from that of the first insulating film;

(4) removing selectively the first insulating film over the second active region with the etching process by utilizing difference in the etching property of the second insulating film;

(5) converting the second insulating film over the first active region into a third insulating film with the thermal oxidation process and forming a fourth insulating film over the second active region;

(6) depositing a conductive material layer and forming respectively a first gate electrode and a second gate electrode over the first and second active regions by patterning the conductive material layer; and

(7) forming respectively a source and drain region within the surface regions of the first and second active regions.

[Claim 2]

The method of manufacturing MOS semiconductor device according to claim 1, wherein the second insulating film is an insulating film including nitrogen.

[Claim 3]

The method of manufacturing MOS semiconductor device according to claim 1, wherein the step (3) is the process in which an oxide film formed with direct nitridation or thermal oxidation of a substrate is nitrided.

[Claim 4]

The method of manufacturing MOS semiconductor device according to any of claims 1 to 3, wherein the step (3) is performed under the gas atmosphere including nitrogen (N) and deuterium (D).

[Claim 5]

The method of manufacturing MOS semiconductor device according to any of claims 1 to 4, wherein the step (4) is performed with the wet method.

[Claim 6]

The method of manufacturing MOS semiconductor device according to any of claims 1 to 4, wherein the step (4) is performed using a solution including hydrogen fluoride (HF) as an etchant.

[Claim 7]

The method of manufacturing MOS semiconductor device according to any of claims 1 to 6, wherein the third insulating film is thinner than the fourth insulating film.

[Claim 8]

The method of manufacturing MOS semiconductor device according to any of claims 1 to 6, wherein the third insulating film has the thickness of 2.0 nm or less, while the fourth insulating film has the thickness of 2.5 nm or more.

[Claim 9]

The method of manufacturing MOS semiconductor device according to any of claims 1 to 8, wherein a threshold voltage of a MOS transistor formed in the first active region is lower than a threshold voltage of a MOS transistor formed in the second active region.

[Claim 10]

The method of manufacturing MOS semiconductor device according to any of claims 1 to 9, wherein impurity ion is implanted through the first insulating film in order to adjust a threshold voltage of a transistor prior to the step (2) after the step (1).

[Claim 11]

The method of manufacturing MOS semiconductor device according to any of claims 1 to 10, wherein a fifth insulating

film having a high dielectric constant is formed over the fourth insulating film prior to the step (6) after the step (5).

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to a method of manufacturing MOS semiconductor device and particularly to a method of forming MOS transistor including gate insulating films of different kinds of thickness.

[0002]

[Prior art]

With diversification of application devices to which semiconductor integrated circuits are mounted, the circuits having different functions such as DRA or SRAM and logic circuit, and CPU within the logic circuit and input and output interface or the like are often mixed in the mounting into the same semiconductor chip. In this case, the circuits emphasized in low current consumption and the circuits emphasized in high speed operation are mixed. Meanwhile, further improvement in high packing density and ultra-fine integration is realized. Therefore, thickness of a gate insulating film has been gradually reduced in the MOS semiconductor device in accordance with the scaling rule.

[0003]

The CMOS used for the circuits emphasized in low power consumption is configured using a transistor which is set to a higher threshold voltage in view of reducing a standby current due to sub-threshold leak. Hence, when the gate insulating film is reduced in the thickness in accordance with the scaling, a gate leak current based in direct on the tunnel phenomenon can be observed. For example, when film thickness is set to 1.9 nm or less, a gate leak current flows exceeding an off current (1.0 pA/μm) of a high threshold voltage transistor and therefore the gate leak current determines a standby current, not attaining the object of low power consumption. Therefore, it is no longer possible to reduce the thickness of the gate insulating film of a high threshold voltage transistor in the low power consumption circuit to about 2.5 nm or less.

[0004]

Meanwhile, the threshold voltage is set to a lower value in the transistor emphasized in high speed operation. In this case, since gate leak occupies only a small ratio, film thickness can be reduced up to 2.0 nm or less. Accordingly, drain current can be improved. Therefore, it is required, for realization of mounting of the low power consumption circuit and high speed operation circuit into one chip of LSI or CMOSLSI, to form the gate insulating films of two kinds of thickness. When the gate insulating film is reduced in thickness, there occur problems of penetration of impurity

(particularly boron atoms) and deterioration in resistance for hot carrier. Here, it is known that use of silicon nitride film is preferential for prevention of penetration of impurity and the silicon nitride film has higher hot carrier resistance than that of silicon oxide film. Accordingly, the silicon nitride film or an insulating film including this silicon nitride film is used for a thin gate insulating film.

[0005]

Fig. 3 shows cross-sectional views of the conventional manufacturing steps of MOS semiconductor device including the gate insulating films of two kinds of thickness which has been disclosed in the Japanese Unexamined Patent Publication No. 1992-154162. First, as illustrated in Fig. 3(a), an element isolating and insulating film 12 is formed over a semiconductor substrate 11, element regions are segmented, and a first silicon oxide film 13 is formed in each element region with the thermal oxidation method. Subsequently, as illustrated in Fig. 3(b), the heat treatment is performed under the N_2 gas or NH_3 gas atmosphere to nitride the entire part of surface. Thereafter, thermal oxidation process is performed only for a short period of time for equalization of film quality. As described above, a first silicon oxide film 13 is changed, by the nitridation process, to a nitrided first silicon oxide film 14 to be used as a first gate insulating film. Next, as illustrated in Fig. 3(c), the element regions in the left side

are covered with a photoresist film 15 and the element regions in the right side and the nitrided first silicon oxide film 15 in the periphery of above element regions are removed, for example, using fluoric acid with the photoresist film 15 used as a mask.

[0006]

Next, as illustrated in Fig. 3(d), a second silicon oxide film which will become a second gate insulating film is formed in the element regions in the right side with the thermal oxidation process. In this timing, the nitrided first silicon oxide film 14 is almost not oxidized and thickness of this film almost does not increase. Subsequently, as illustrated in Fig. 3(e), a gate electrode 17 formed of polycrystalline silicon is respectively formed over the first gate insulating film and the second gate insulating film. Next, as illustrated in Fig. 3(f), a diffusing layer 18 which will become the source and drain is formed, the entire surface is covered with an interlayer insulating film 19, and thereafter a contact hole is bored thereto. Thereafter, a wiring electrode 20 connected to the diffusing layer 18 is formed and the entire surface thereof is covered with a cover insulating film 21. As described above, the thickness of the first gate insulating film almost does not give any influence on the step to form the second gate insulating film. Accordingly, the second gate insulating film can be formed thicker than the first gate insulating film.

[0007]

[Problem to be Solved by the Invention]

In the conventional method of forming the gate insulating films of two kinds of thickness, the first gate insulating film over one element regions are covered with the photoresist film and the insulating films over the other element regions are removed by the etching process. However, in this method, migration of impurity to the first gate insulating film from the photoresist cannot be avoided. Moreover, damages will be given to the gate insulating films with peeling of the photoresist film and subsequent washing process. In the gate insulating film in which thickness is extremely reduced to about 2 nm or less, film quality of the gate insulating film is greatly influenced by the steps described above and it is no longer possible to attain uniformity in the characteristics and reliability in the product. A subject of the present invention is to solve the problems in the prior art and the object of the present invention is to attain uniformity in quality of the gate insulating film and reliability of product by providing the manufacturing method in which it is not required to cover a gate insulating film with a photoresist film.

[0008]

[Means for Solving the Subject]

In view of attaining the object described above, the present invention can provide a method of manufacturing MOS semiconductor device comprising the steps of (1) covering respectively the surfaces of a first active region and a second active region segmented with an element isolating and insulating film with a first insulating film, (2) removing selectively the first insulating film over the first active region with the etching process, (3) forming a second insulating film over the first active region with a material having the etching property which is different from that of the first insulating film, (4) removing selectively the first insulating film over the second active region with the etching process by utilizing difference in the etching property of the second insulating film, (5) converting the second insulating film over the first active region into a third insulating film with the thermal oxidation process and forming a fourth insulating film over the second active region, (6) depositing a conductive material layer and forming respectively a first gate electrode and a second gate electrode over the first and second active regions by patterning the conductive material layer, and (7) forming respectively a source and drain region within the surface regions of the first and second active regions.

[0009]

Preferably, the second insulating film is formed of silicon nitride film. Moreover, the step (3) is preferably performed with the direct nitridation under the gas atmosphere including nitrogen (N) and deuterium (D). Moreover, the step (4) is preferably performed with a wet method.

[0010]

[Preferred Embodiments]

Next, the embodiments of the present invention will be described in detail with reference to the accompanying drawings.

[First Embodiment]

Fig. 1 shows cross-sectional views of manufacturing steps of the manufacturing steps in a first embodiment of the present invention in which a MOS transistor having a low (small absolute value) threshold voltage and a MOS transistor having a high (large absolute value) threshold voltage are formed over the same semiconductor chip.

[0011]

First, an element isolating and insulating film 2 is formed in the thickness of 350 nm with a trench method and then a first silicon oxide film 3 is also formed in the thickness of 20 nm with the thermal oxidation method over a semiconductor substrate 1 formed of silicon as illustrated in Fig. 1(a). Thereafter, the B ion is implanted to adjust the threshold voltage of MOSFET using the first silicon oxide film as a cover

oxide film. Next, as illustrated in Fig. 1(b), a region to form the MOS transistor having a high threshold voltage (hereinafter, referred to as high Vth region) is covered with a photoresist film and a first silicon oxide film 3 over the region to form the MOS transistor having a low threshold voltage (hereinafter, referred to as low Vth region) is removed with the etching process using the photoresist film as a mask. After the resist mask is peeled, the heat treatment is performed for 30 seconds under 1000°C within the NH_3 gas atmosphere for nitridation of the surface of silicon substrate over the low Vth region as illustrated in Fig. 1(c). With this nitridation process, a silicon nitride film 4 is formed in the thickness of 1 nm over the low Vth region. Meanwhile, nitrogen atoms are also mixed to the surface of the first silicon oxide film 3 remaining over the high Vth region.

[0012]

Next, as illustrated in Fig. 1(d), the silicon oxide film 3, to which nitrogen atoms are mixed, remaining over the high Vth region is removed by the etching process using buffered fluoric acid. In this timing, the silicon nitride film 4 remaining over the surface of the silicon substrate of the low Vth region is not etched. Subsequently, in order to form a gate insulating film, the heat treatment is performed for 60 seconds under 1000°C in the oxygen atmosphere. As a result, as illustrated in Fig. 1(e), a second silicon oxide film 5 is

formed over the substrate surface of the high Vth region, while a silicon oxide film 6 including nitrogen is formed over the substrate surface of the low Vth region. In this case, a film forming rate in the low Vth region becomes slower than that of the high Vth region because the silicon nitride film 4 exists. As a result, a difference is generated in the film thickness. Film thickness of the second silicon oxide film 5 over the high Vth region is 2. 8 nm in one hand but film thickness of the silicon oxide film 6 including nitrogen over the low Vth region becomes 1.8 nm on the other hand. Subsequently, as illustrated in Fig. 1(f), a gate electrode 7 is formed by depositing the polycrystalline silicon conforming to the manufacturing process of an ordinary CMOSLSI and an impurity diffusing layer 8 which will become the source and drain region is formed with ion implantation.

[0013]

[Second Embodiment]

In the second embodiment, for the nitridation process of the silicon substrate described with reference to Fig. 1(c) of the first embodiment described above, the ND_3 (a substance obtained by substituting deuterium for hydrogen within the NH_3 molecules) gas is used in place of the NH_3 gas. This ND_3 gas is used for enhancing hot carrier resistance of a device. The mechanism is that since deuterium is fetched into the gate insulating film over the low Vth region, the Si-H coupling which

can be easily cut with the hot carrier is changed to the Si-D coupling which cannot be cut easily.

[0014]

[Third Embodiment]

Fig. 2 shows cross-sectional views of manufacturing steps in a third embodiment of the present invention. Since the processes of Figs. 1(a) and 1(b) in the first embodiment are also performed in this second embodiment, the same illustration and description are omitted here. After completion of the step of Fig. 1(b), the silicon nitride film 4 is formed in the thickness of 1 nm over the silicon substrate of the low Vth region with the nitridation process for 30 seconds under 1100°C in the N_2 gas atmosphere as illustrated in Fig. 2(a). Next, as illustrated in Fig. 2(b), the silicon oxide film 3 remaining over the high Vth regions removed by the etching process using the buffered fluoric acid. In this case, the silicon nitride film 4 existing over the silicon substrate surface of the low Vth region is not etched. Next, the second silicon oxide film 5 is formed in the thickness of 2. 5 nm over the silicon substrate surface of the high Vth region, while the silicon oxide film 6 including nitrogen is formed in the thickness of 1. 5 nm over the substrate surface of the low Vth region as illustrated in Fig. 2(c) with the heat treatment for 60 seconds under 800°C in the wet oxygen atmosphere.

[0015]

Next, the high dielectric constant film 9 is formed over the silicon oxide film 6 including nitrogen and the second silicon oxide film 5 by depositing a tantalum oxide (Ta_2O_5) in the thickness of 1 nm using the CVD method as illustrated in Fig. 2(d). Subsequently, a multilayer conductive film 10 is formed by respectively depositing polysilicon in the thickness of 15 nm, tungsten nitride (WN) of 10 nm, and tungsten (W) of 10 nm as illustrated in Fig. 2(e). Thereafter, as illustrated in Fig. 2(f), the multilayer conductive film 10 is patterned to form a gate electrode 7 and ion implantation is performed to form an impurity diffusing layer 8 which will become the source and drain region.

[0016]

The preferred embodiments of the present invention have been described above. However, the present invention is not limited thereto and allows various changes and modifications as required within the scope not departing from the subject matter of the present invention. For example, the gate electrode may be formed of a high melting point metal film or a laminated film of polycide film or polysilicon and high melting point metal. Moreover, the oxide film and high dielectric constant film deposited over the acid nitride film may be formed of the other high dielectric constant material such as TiO_2 in place of the tantalum oxide film. In addition, the substrate has been nitrided in direct to form a nitride film

in the preferred embodiments described above, but it is also possible that the thermal oxidation is performed first and then nitridation process is performed to a thermal oxide film. Moreover, the dry method using HF gas or the like may be used in place of the method to remove the third silicon oxide film with the wet method. Furthermore, materials and numerical data described in the preferred embodiments are only examples and the present invention is not limited thereto.

[0017]

[Effects of the Invention]

According to the present invention, as described above in detail, since the gate insulating films of different kinds of thickness can be formed without covering the gate insulating films with the photoresist film, the gate insulating film is not contaminated by the photoresist. Moreover, the gate insulating film is never damaged by the peeling and washing processes of the photoresist. Therefore, according to the present invention, the thin gate insulating film may be formed with higher reproducibility and reliability. In addition, the semiconductor device comprising a high threshold voltage MOSFET including a comparatively thick gate insulating film and a low threshold voltage MOSFET including a comparatively thin gate insulating film can be provided with higher reliability.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

Cross-sectional views of processing steps in the manufacturing methods of the first and second embodiments of the present invention.

[Fig. 2]

Cross-sectional views of processing steps in the manufacturing method of the third embodiment of the present invention.

[Fig. 3]

Cross-sectional views of processing steps in the conventional manufacturing method.

[DESCRIPTION OF THE REFERENCE NUMERALS]

1: Semiconductor substrate;

2: Element isolating and insulating film;

3: First silicon oxide film; 4: Silicon nitride film;

5: Second silicon oxide film;

6: Silicon oxide film including nitrogen;

7: Gate electrode; 8: Impurity diffusing layer;

9: High dielectric constant film; 10: Multilayer conductive film;

11: Semiconductor substrate;

12: Element isolating and insulating film;

13: First silicon oxide film;

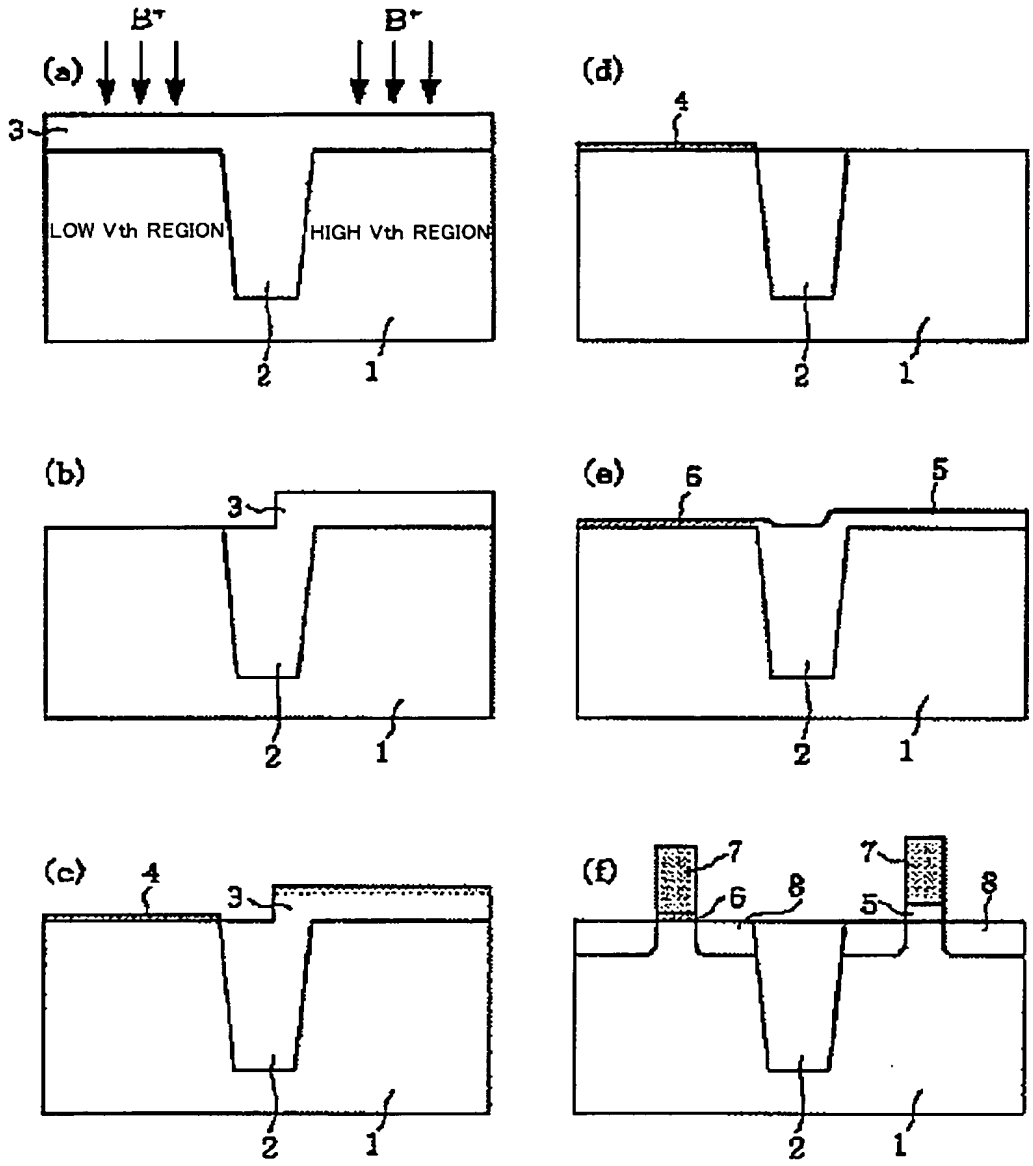
14: Silicon oxide film including nitrogen;

15: Photoresist film; 16: Second silicon oxide film;

17: Gate electrode; 18: Diffusing layer;

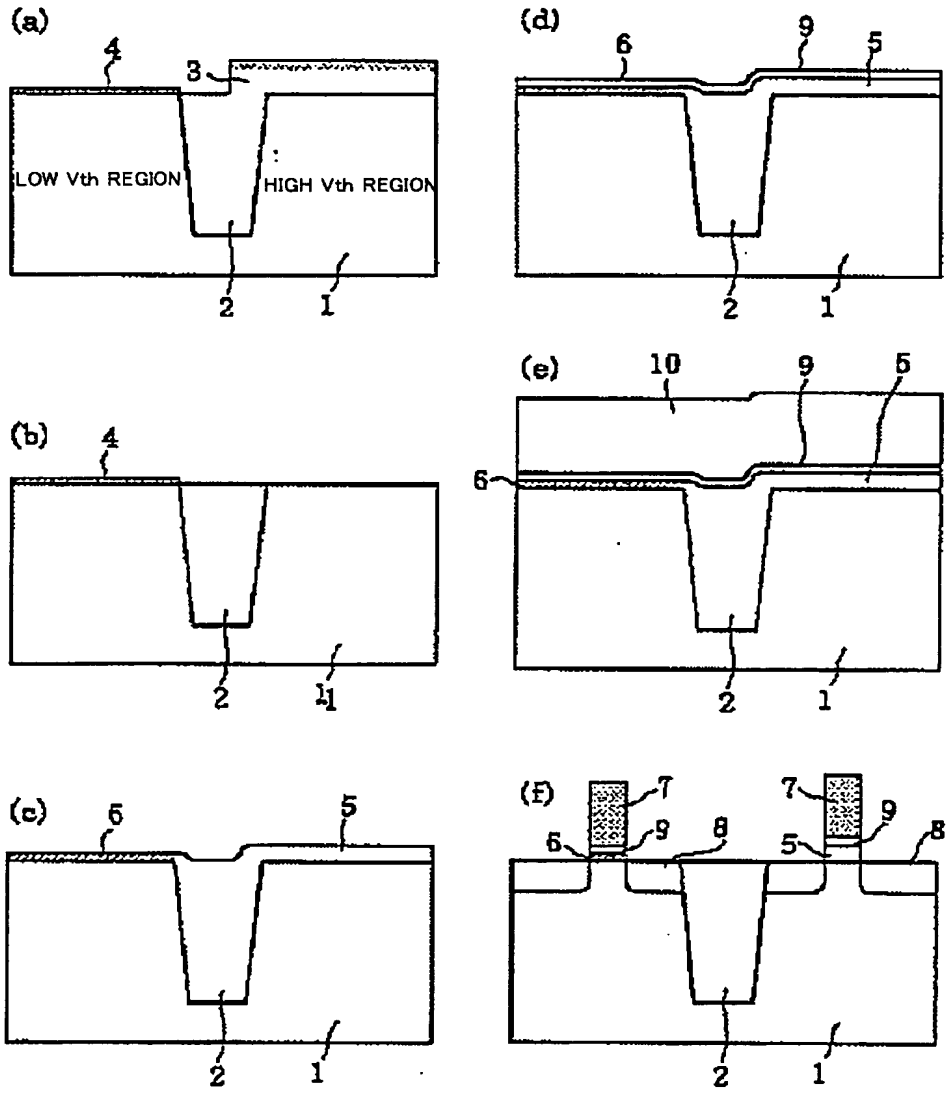
19: Interlayer insulating film; 21: Cover insulating film.

FIG. 1



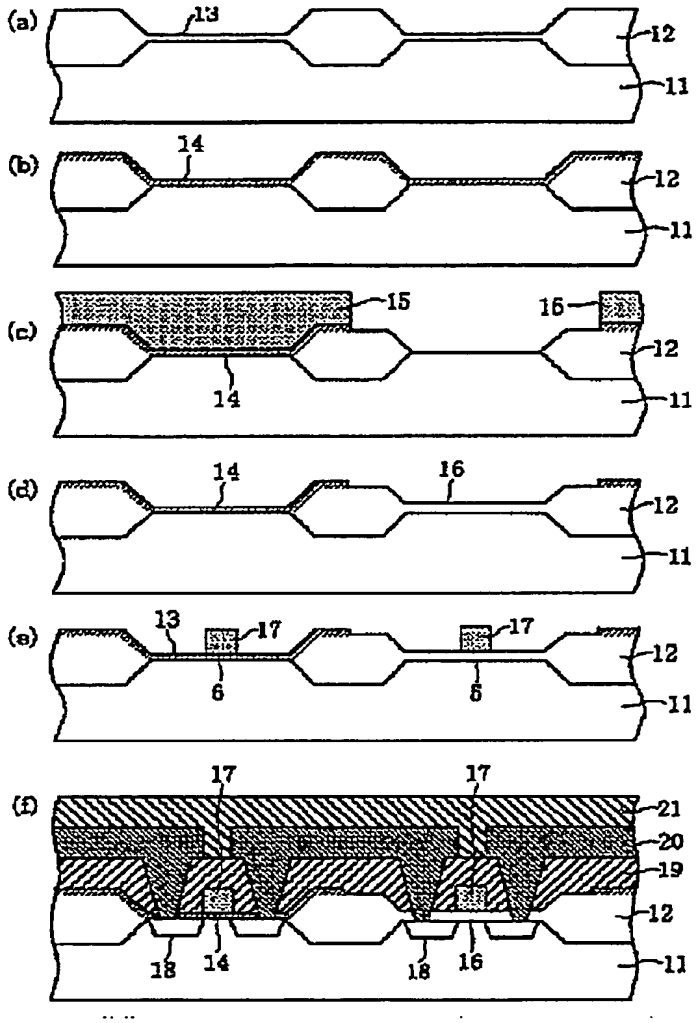
1: SEMICONDUCTOR SUBSTRATE
2: ELEMENT ISOLATING AND INSULATING FILM
3: FIRST SILICON OXIDE FILM
4: SILICON NITRIDE FILM
5: SECOND SILICON OXIDE FILM
6: SILICON OXIDE FILM INCLUDING NITROGEN
7: GATE ELECTRODE
8: IMPURITY DIFFUSING LAYER

FIG. 2



1: SEMICONDUCTOR SUBSTRATE
2: ELEMENT ISOLATING AND INSULATING FILM
3: FIRST SILICON OXIDE FILM
4: SILICON NITRIDE FILM
5: SECOND SILICON OXIDE FILM
6: SILICON OXIDE FILM INCLUDING NITROGEN
7: GATE ELECTRODE
8: IMPURITY DIFFUSING LAYER
9: HIGH DIELECTRIC CONSTANT FILM
10: MULTILAYER CONDUCTIVE FILM

FIG. 3



11: SEMICONDUCTOR SUBSTRATE
12: ELEMENT ISOLATING AND INSULATING FILM
13: FIRST SILICON OXIDE FILM
14: SILICON OXIDE FILM INCLUDING NITROGEN
15: PHOTORESIST FILM
16: SECOND SILICON OXIDE FILM
17: GATE ELECTRODE
18: DIFFUSING LAYER
19: INTERLAYER INSULATING FILM
20: WIRING ELECTRODE
21: COVER INSULATING FILM